

CLAIMS:

1. An integrated circuit for sampling outputs representing a pixel value comprising:

- (a) two first variable capacitors each having a variable range of capacitance and each for receiving a voltage representing the pixel value;
- (b) two first transistors respectively connected electrically to each of the first variable capacitors for transferring a voltage to each of the variable capacitors; and
- (c) two second transistors respectively connected electrically to each of the first variable capacitors for transferring the voltage from each of the first variable capacitors.

2. The integrated circuit as in claim 1 further comprising two second capacitors each having a variable range and respectively connected electrically to the first variable capacitors for receiving voltage from the first variable capacitors when the second transistor is pulsed.

3. The integrated circuit as in claim 2 further comprising a differential amplifier for receiving the voltage from the two second capacitors for determining a resultant absolute voltage.

4. An integrated circuit for collecting incident light that is converted into a charge and for sampling the charge, the integrated circuit comprising:

- (a) an image sensor for receiving the incident light which is converted into the charge;
- (b) two first variable capacitors each having a variable range of capacitance and each for receiving a voltage from the image sensor;
- (c) two first transistors respectively connected electrically to each of the first variable capacitors for pulsing the voltages to each of the first variable capacitors; and

5. The integrated circuit as in claim 4 further comprising two second capacitors each having a variable range and respectively connected electrically to the first variable capacitors for receiving the voltage from the first variable capacitors when the second transistor is pulsed.

6. The integrated circuit as in claim 5 further comprising a differential amplifier for receiving the voltage from the two second capacitors for determining a resultant absolute voltage.